CPRE 4920 Status Report 02

12/18/2025 – 02/04/2026

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Cache Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

This week we continued to work on our design implementation and additional software that will be used for the final tapeout.

- **Past Week Accomplishments**
    - Colin McGann: Worked on textures and FPGA integration
    - Jack Tonn: inquired verification practices with industry professionals & da core
    - Dawud Benedict: Again, fixed cache HDL. Near finished with unit test
    - Michael Drobot: Wishbone reg refactor, datasheet reg layouts, VGA framebuffer read modifications
    - Sam Forde: Fixed all of the issues in the hardening flow for commercial SRAM.
    - Josh Arceo: Worked on optimizing the optimizer. Now quits early on magic run.
    - Emil Kosic: Completed HDL for the wb to pk bus, currently testing it

- **Pending Issues**
    - Core implementation
    - Core controller test

- FPGA Working

- **Individual contributions**

NAME	Individual Contributions	Hours this period	HOURS cumulative
Colin McGann	Continued work on FPGA integration and textures	20	250
Jack Tonn	Core synthesis & high level design	10	200
Dawud Benedict	HDL and testing	15	113
Michael Drobot	Core controller & wishbone reg	30	262
Sam Forde	Got SRAM to harden in Caravel	8	95
Josh Arceo	Optimized optimizer	7	87
Emil Kosic	HDL for wb to pk and testing	7	96

- **Plans for the upcoming weeks**
  - Colin McGann: Fix the SPI mem for FPGA and work on the SPI chip model
  - Jack Tonn: Implement verification methods from industry professionals and core
  - Dawud Benedict: Finish unit testing. Hopefully, probably, maybe it will work and I can move on otherwise make it work
  - Michael Drobot: Core controller testbench
  - Sam Forde: Either work on the SPI chip model or find a new part to work on
  - Josh Arceo: Finally make area tables
  - Emil Kosic: wrap up wb to pk testing